Trends in Life Sciences
An International Peer-reviewed Journal
ISSN: 2319–4731 (p); 2319–5037 (e)

DESIGNING 10 TRANSISTOR FULL – ADDER AXIS BASED ON XOR GATE OPTIMIZE CONSUMPTION ABILITY AND ITS SIMULATION BY APPLYING MICROWIND SOFTWARE

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ABSTRACT
Adder is considered as one of the important components of processors and the most important component in CPU, Adder Logic Unit and Digital Signal Process. So, improving adder axis designing with law ability and high efficiency is very important. Because this leads to reduce electronic devices consumption, just a few numbers of different kinds of full- adders are represented in literatures which are based on static and dynamic designing methods. All usual adder axises are applied in static CMOS. Technology via 28 transistors and by developing the design of a new adder which is called Static Energy Recovery Full Adder using transistors is applied.That has the least number of transistors and is introduced as the least consumed axis. Most of the less consumption adders like SERE are applied by crossing transistors and despite of the low consumption they have drop problem, because of this, they aren't used broadly. Considering this fault, there are important factorsin making more complex axises like collectors. At present study, a new approach is offered to design full adder axis which is based on XOR gate and has low consumption ability and high axis speed and very effective in improving the function of these basic blocks. After representing designing approach and the details about how it works, we will compare that with some new designs which are simulated by Microwind software, in this case.

KEYWORDS: Full Adder, XOR gate, Microwind Software.

INTRODUCTION

Through passing years and development of technology and science, human needs to get more information with high speed processing and then saving them which are increasingly grow up. Gordon mour senior assistant in Intle Company 1965 represent an idea that per 18 months, the number of transistor which work for each chip is twice and chip axis is also half of the previous size. Adder is a main processor unit which is used abundantly in all computer central processors. Adder is also is used a lot in other electronic devices such as calculator and also portable electronic devices on which consumption ability is one of the most important parameters. In this article we will introducten all 10 transistors full- adder with low consumption ability and high efficiency based on XOR gate (Wairya *et al., 2011).*

DIFFERENT AXISES

After1959 that first digital adding axis appeared, different companies designed these seri of axises and sent them to electronic markets among which some of them attracted a lot of electronic engineers and this led other electronic device manufactures to produce similar axises and in order to sell their products, they used codes which were like those were used by primary originators. The case of coping gradually disappeared and such kind of adding axises were called a big family of digital axises. For example we can name Texas Instrument company which initiated TTL adding axises that named his first product SN7400 that included NAND 4 gates and after that gave its IC similar names as SN 7401, SN 7402 Etc (Ewert., 2009).

Synthetic Axises designing

The most important synthetic axises are listed in table 1 have design method of synthetic axises first specify the entrances and exits from the features and definitions of the problem. In the second stage correct table is created and specify the relationship between entrances and exits, then in the third stage simplify the axis using Karnaugh table. In the fourth stage track the magical diagram of the axis and finally in the last stage research to confirm the correctness of your design. (Pedrycz and Reformat, 2006).

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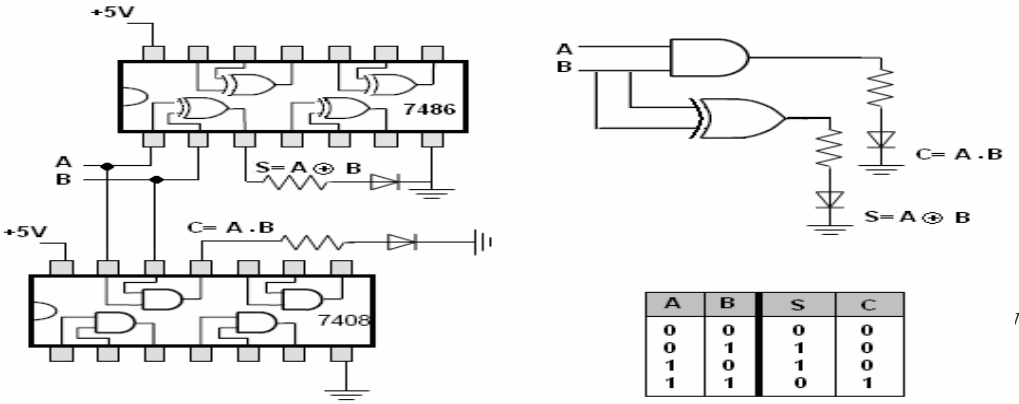
Table 1: the most important synthetic axises

Row	Title	Function
1	Adders	Collector
2	Sub tractors	Sub racting
3	Comparators	Comparing
4	Decoders	Decoding
5	Encoders	Encoding
6	Multiplexers	multiplexing

Half – Adder Axis designing

A half- adder id an axis that adds two 2×2 numbers. The reason of calling this axis so is that this axis is not able to add three numbers, two main numbers, two main numbers whit a carry number from previous add(Ghaznavi-Ghoushchi and Nabavi,2002).

This axis has to exist on is sum and the other is carry number and is axis is like what is shown in figure 1.



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Main Ol

Among ' /hich should be consider

Table 2.

Reducing the number of gates	Reducing the expenses
Design simplicity	Increasing the speed

Fallowing we will introduce some logical axises along with Karnaugh table and Karnaugh is shown in figure 2 (Balasubramanian, 2007). Finally considered IC which is used in adder axises are a evaluated (Pedrycz and Reformat, 2006).

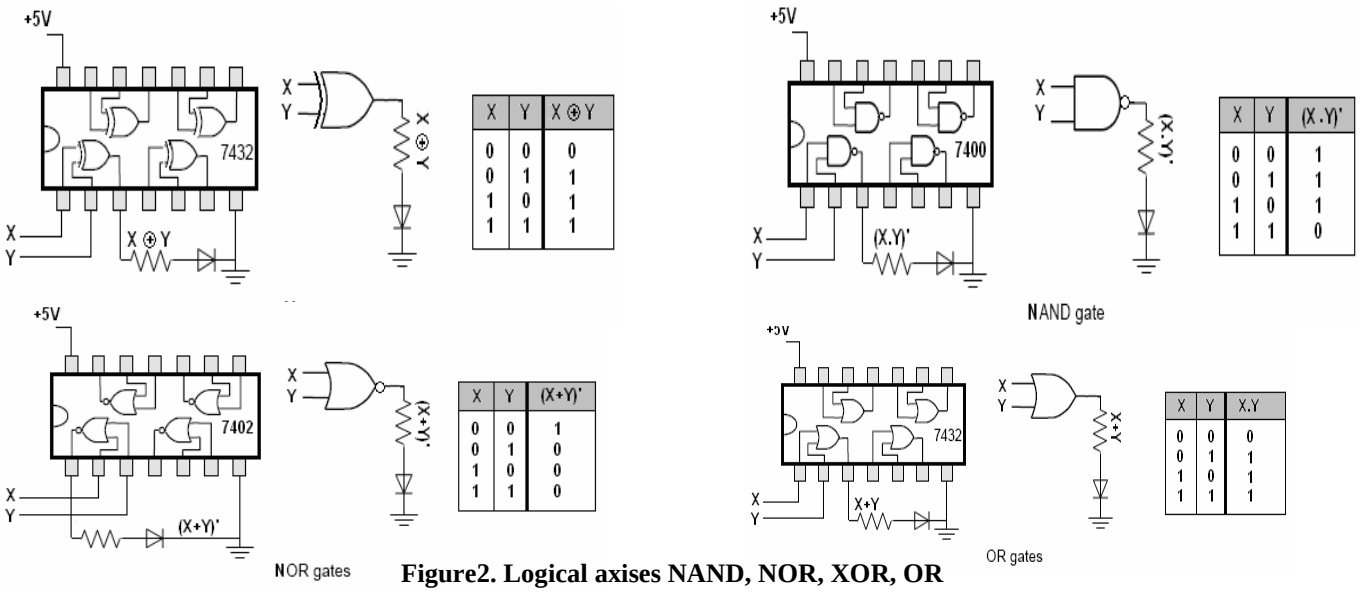


Figure2. Logical axises NAND, NOR, XOR, OR

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Consumption a Bility in a CMOS axis

$$P_{total} = p_{switching} + p_{short-circuit} + p_{liakage}$$

Where:

$p_{switching}$ is the switching ability. This ability is used during charging and recharging of capacitor.
$p_{short-circuit}$ is the short connection ability and because of the existence of the circuit between Vdd and the hand is used while switching transistor.
$p_{liakage}$ is static ability and it happens when there is a leakage or static circuits.

REDUCE THE CONSUMPTION ABILITY IN FULL – ADDER AXISES

Reducing consumption ability in full – adder axises presented approaches in table 2 are proposed to reduce the consumption ability in full – adder axises.

Table 2. Strategics to Reduce the Consumption Ability in full- adder axises.

Row	Explanations
1	Reducing entrance and exit capacities which lead to reduce the dynamic ability. So less nodes should ne connected to (out and sum) signal
2	The most important part of consumption ability in a full- adder axis are XNOR and XOR gates. So the number of transistors and consumption ability of this part should be reduced.
3	Simultaneous use of GND and Vdd should be prevented which leads to reduce short connection and static ability
4	Reducing the number of transistors usually leads to reduce the consumption ability
5	Preventing the use of inventers which leads to reduce the static ability

REVIEWING FULL-ADDER AXISES

All full – adders are divided into 2 groups in exit way point of view (Babu, 2003).

- First Group: include full – adder axises which have complete Soing like C-CMOS, TGA, TFA and 14 transistors.
- Second Group: these are full- adder axises which don't have complete Soing like SERE and MBA12T.

Karnaugh table of full- adder axises is represented in table 3 (Wairya *et al, 2011).*

Table 3.Karnaugh table of full – adders

A	B	E	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C-CMOS full- adder axis

This full- adder is based on the usual structure of CMOS which owns 28 transistors (figure (4)) which are located on PUN (Poal Up Network) up transistors on PMOS and in PDN (Poal Down Network) are located on don transistor PDN on NMOS.

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And entrance capacity of the CMOS gate is big since each entrance is connected to one NMOS and PMOS. The main advantage of this axis is that reacts in a resisting way toward voltage changes and transistors' size beside these arrangement of C-CMOS axis is very simple.

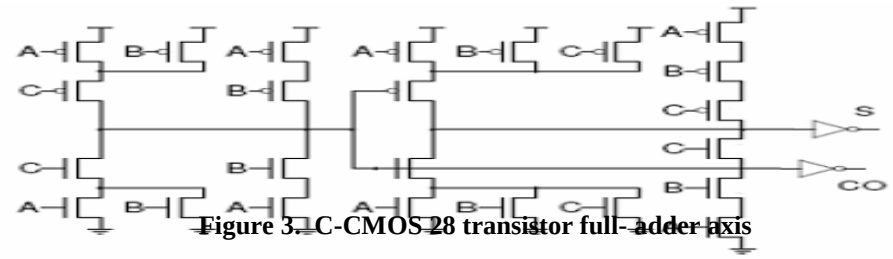

Figure 3. C-CMOS 28 transistor full- adder axis

TGA full- adder axis

This axis is designed based on the gat theory. This full- adder has 20 transistors. This axis has low consumption ability rate naturally. The structure of this axis is based on XOR and XNOR gates, and tow entrance. The structure of TGA full – adder axis is shown in figure4.The main failure of this axis is that it has low drive ability, when TGA and TFA are arranged in a Seri way, their function will be better.

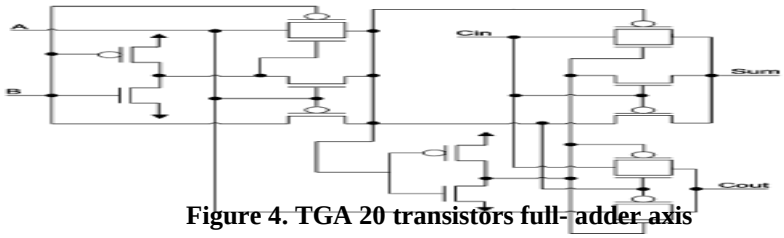

Figure 4. TGA 20 transistors full- adder axis

TFA full- adder axis

This axis contains 20 transistors which lead it to have less consumption rate. TFA full- adder axis is shown in figure 5.

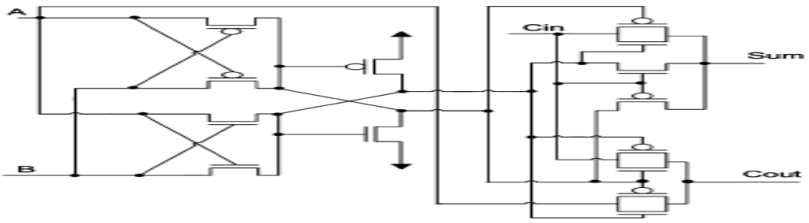

Figure 5. TFA 16 transistor full- adder axis

14 Transistor full- adder axis

This axis has Soing exist voltage. Comparing other mentioned axises, this one occupies little space 14 transistors . full-adder axis is shown in figure 6.

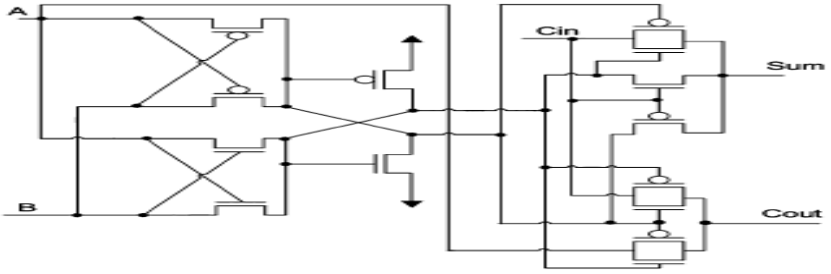

Figure 6. 14 transistor full- adder axis

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MBA full- adder axis

MBA- 12 T axis includes 12 transistors. This full- adder axis designed based on 6 multiplexers. As it can be seen in the picture, this axis doesn't use any land or Vdd, so the consumption rate will decrease. This picture shows that there will be driver's paths which included 3 Seri transistors. In the mentioned paths, the transistors' size should be tripled to balance the exit way and improve the PDP. So, the area for the axis increases. Figure shows a simple multiplexer which used in MBT- IZT transistor. In figure 7 we have presented a MBA full- adder axis.

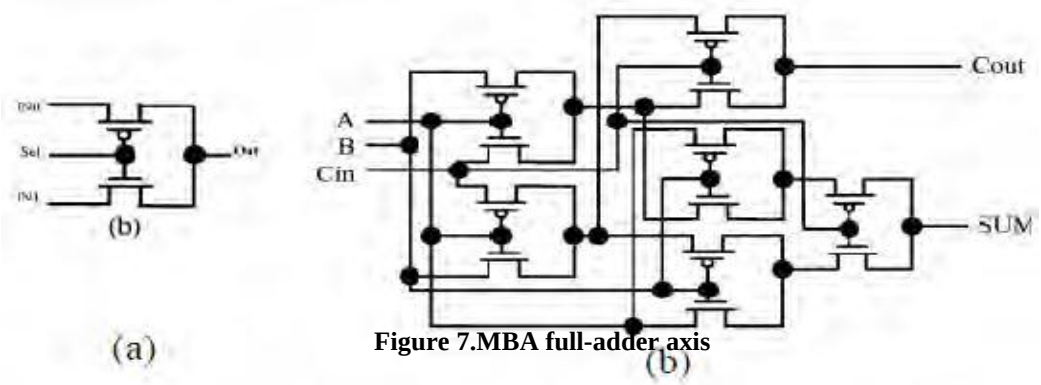

Figure 7.MBA full-adder axis

PROPOSAL AXIS

In most of VLSI applications like digital signal processing. Picture and micro processor processing, math operations are totally used. Adding sub multiplying and MAC are examples of common mathematical operations. 1 bit full- adder cell is the main block of these models and determines the performance of the whole system. Full- adder cell not only plays an important role, but also is the main consumption rate in the system. So, its functioning improvement is necessary for system performance improvement. To design and analyze a full- adder we can divide it to the smaller models. Each of these models can be designed in an optimized way. Most of the full- adder cells are obtained by the connection of these models.

CMOS 1 bit full- adder cells

Full- adder diagram block and its basic blocks are represented in figure 8. At the same time different arises are represented for each model. The structure which is used for designing low art consumption full- adder is to divide the cell into 2 parts which in the former, the middle logical of XOR and XNOR are produced.

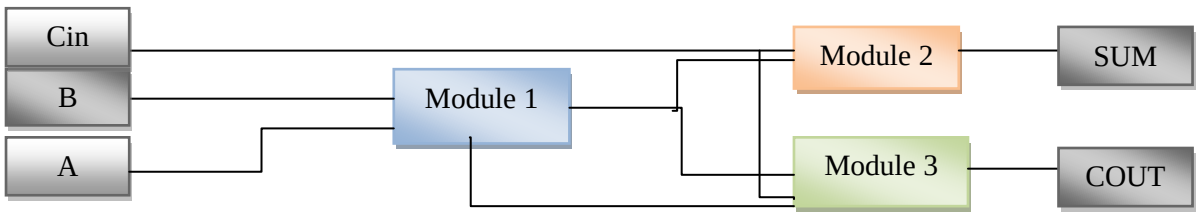

Figure 8. full- adder diagram block with its basic models

The XOR axis used in the Presented Full-Adder axis

The axis which is shown in figure 9 shows a 4 transistor XOR and the presented full- adder is produced based on this XOR- there is no feeding resource in this axis and because of this static rate is reduced (Keivan *et al.,2009*).

High speed PMOS transistors increase the axis speed in 3 entrance state. When C= B=1, both of PMOS transistors are turned off and NMOS block is on. Both NMOS transistors are series so the delay to recharge the exit way is increased. If C=B=O, then the exit way has the threshold problem and the exit voltage equals to Vt,PMOS transistor doesn't cross zero completely. The most important failure in this XOR is the exit way Voltage reduction. Consumption rate reduction and transistor number reduction are two of the most important features of this axis. Proposal logic to design this full – adder is made of one XOR gate and tow multiplexer to make sum and count functions. Reduction of the number of XOR gate leads to the reduction of consumption rate. This logical is shown in the fallowing figure.

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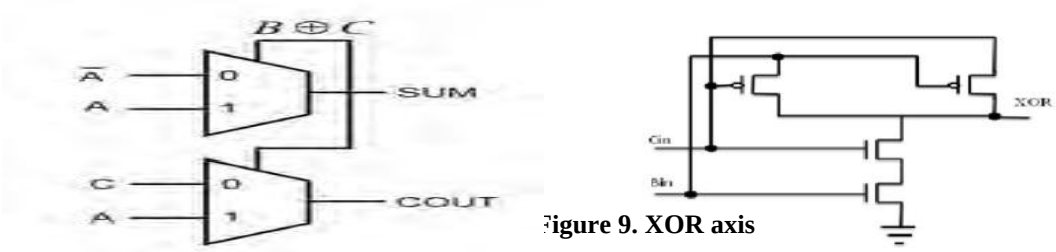

Figure 9. XOR axis

New Proposal full- adder axis

As shown in the figure 10, the presented axis has just one XOR gate and two multiplexer to make a full- adder. XOR gates have the most rates in one full- adder. By reducing one XOR axis, the total consumption rate reduces. As it's sown in the picture, XOR signal is used as one static two multiplexer selector. XOR signal has voltage as much as Vt. Multiplexer exit way will have the problem of threshold voltage as much ad VT So like SERF; this model has the threshold voltage. XOR mediator signal s\drives PMOS transistor gate and NMOS two gate transistor. In the above axis, two multiplexers create cout and sum signals that both of them consist of two transistors.

In figure 10, we see no vdd and no land on this axis (Chang and Zhang, 2005).

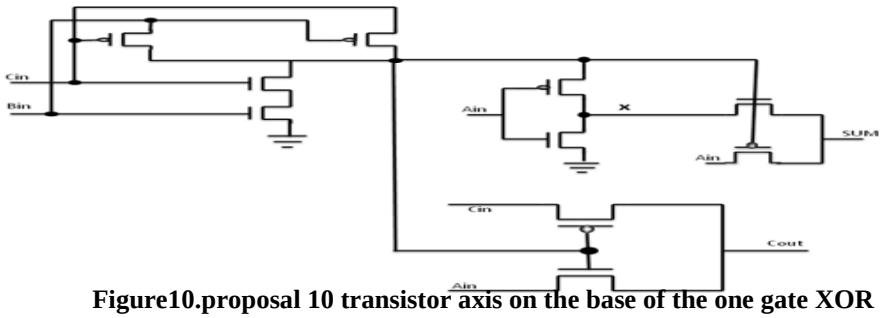

Figure10.proposal 10 transistor axis on the base of the one gate XOR

Therefore this part also leads to reduce consumption rate. The simplify of manufacturer axises of sum and cout is the other reason to reduce the consumption rate and delay in this axis. There is a semi- inventor axis in this full – adder axis to reverse a entrance. This inventor should work just when XOR signal equals to 1. So we use XOR signal as the feeding resource to reduce the short connection and leakage circuits it means that switching operation in X node, because of the XOR signal in the inventor will be decreased (Chang and Zhang ,2005).

Benefits of This Axis over Other Proposed Ones

benefits of this axis comparing other proposal ones the main point about all adder axises is that, since Full- Adder cells are always closed after each other as cascade to form an account axis, their drivability should be valid. A driving cell should provide full swing exit to drive other next cells. Nonetheless, the performance of the axis will be reduced and won't work correctly in low voltage. Benefit of this axis comparing other proposal axises includes (Keivan *et al., 2009*).

- The number of transistors is reduced in this axis
- Consumption rate is reduced
- Simplify of the axis to be designed

SIMULATION

Proposal full adder axis are simulated by micro wind soft wares and 0.18 micro meter technology, in this axis, both inventors have the same W/L, PMOS transistor size is twice NMOS. The reason to use these two inventors is to make sure that the level of exit voltage is valid. An one bit Full-Adder axis with low consumption rate is introduced in this axis. This Full-Adder is made of one 4 transistor gate where in no feeding resource is used. This axis has the least consumption rate among all ather full- adders. Layout designing using micro wind software is presented in figure 11. Entrance waves in figure 12 and final results are simulated together with entrance wave in figure 13.Comparing results by Karnaugh table we can reach to the correct function of the axis.

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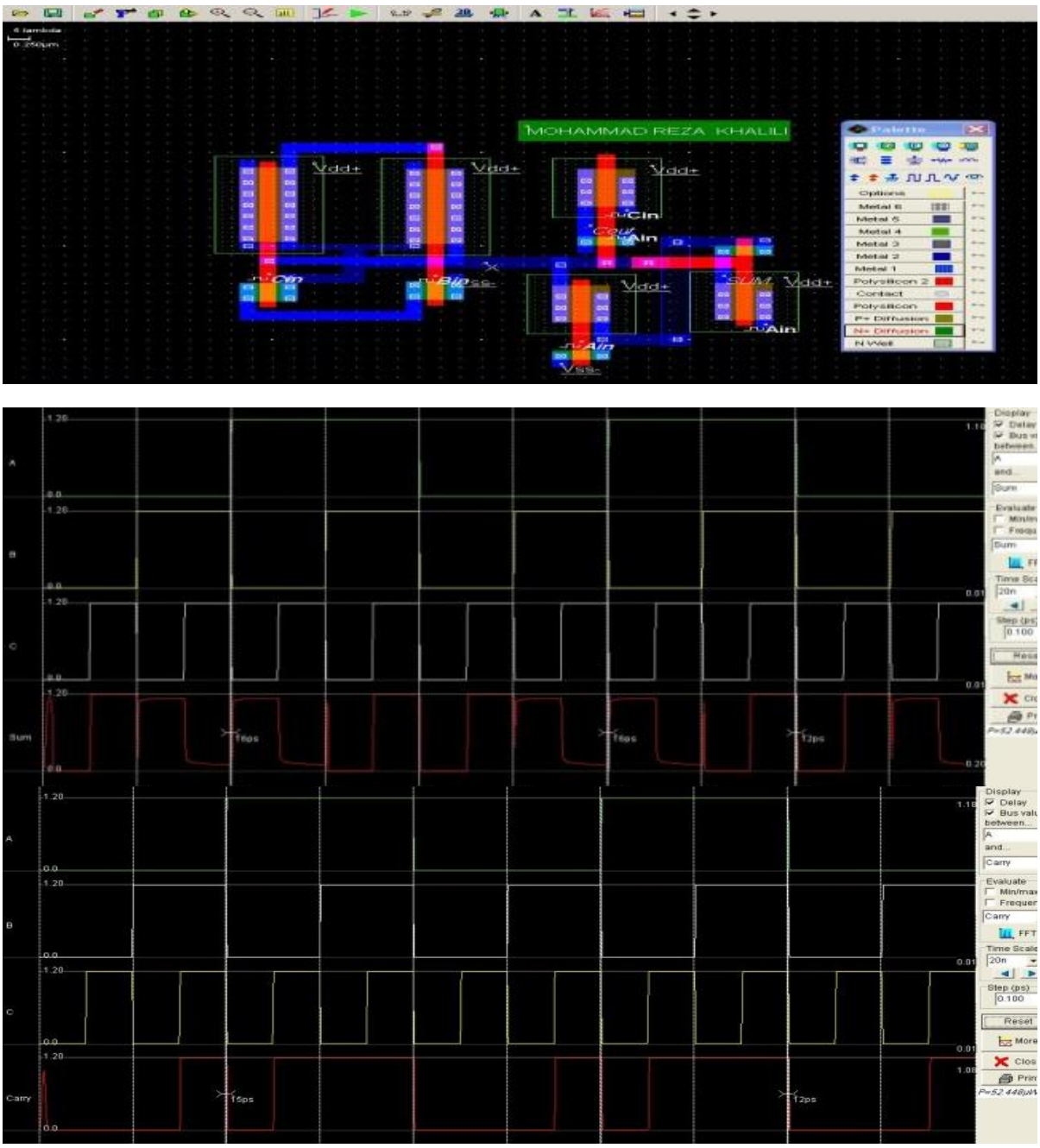

Figure 13. entrance and exit waves sum and carry

CONCLUSIONS

Full- Adder axis is one of the important elements in processors and the most important element in CPU, logical account units and digital signal processing. Considering the increasing growth of the wireless and portable electronic instruments, designing of VLSI axis with performance and low capability, a lot of new and innovated designing are done in this case to run this structure. Full – Adder axis adds two mono bit numbers and if there is any carry number, imports it in the operation. Because of the sensitivity of the Full-Adder, axis the designed axis should have adequate and high speed and its consumption rate should also be low. Considering all of these, along with evaluating other Full-Adder axises, designing 10 transistors Full-Adder based on XOR gate is proposed in the present study. In this

designing, the number of transistors and the consumption rate is reduced and finally its being simple can be one of its advantages. The results of simulation which are done by micro wind software also show the low consumption rate and its validity comparing to karnaugh table.

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